Institute of Microelectronic Systems

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Hardware-Accelerated Design Space Exploration Framework for Communication Systems

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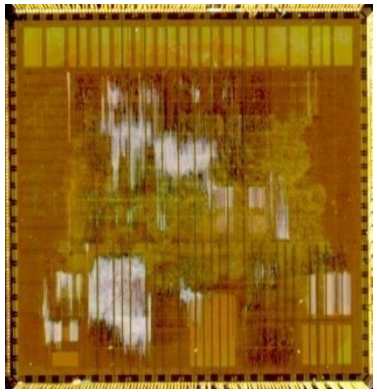
Motivation

- High-throughput SDR systems require application specific digital circuits
- Mobile SDR hardware platforms must provide high processing power at low power consumption
- Advanced and novel signal processing algorithms push the limits of SDR platforms

➔ Goal: provide strategies and environment for designing efficient SDR platforms for future communication systems

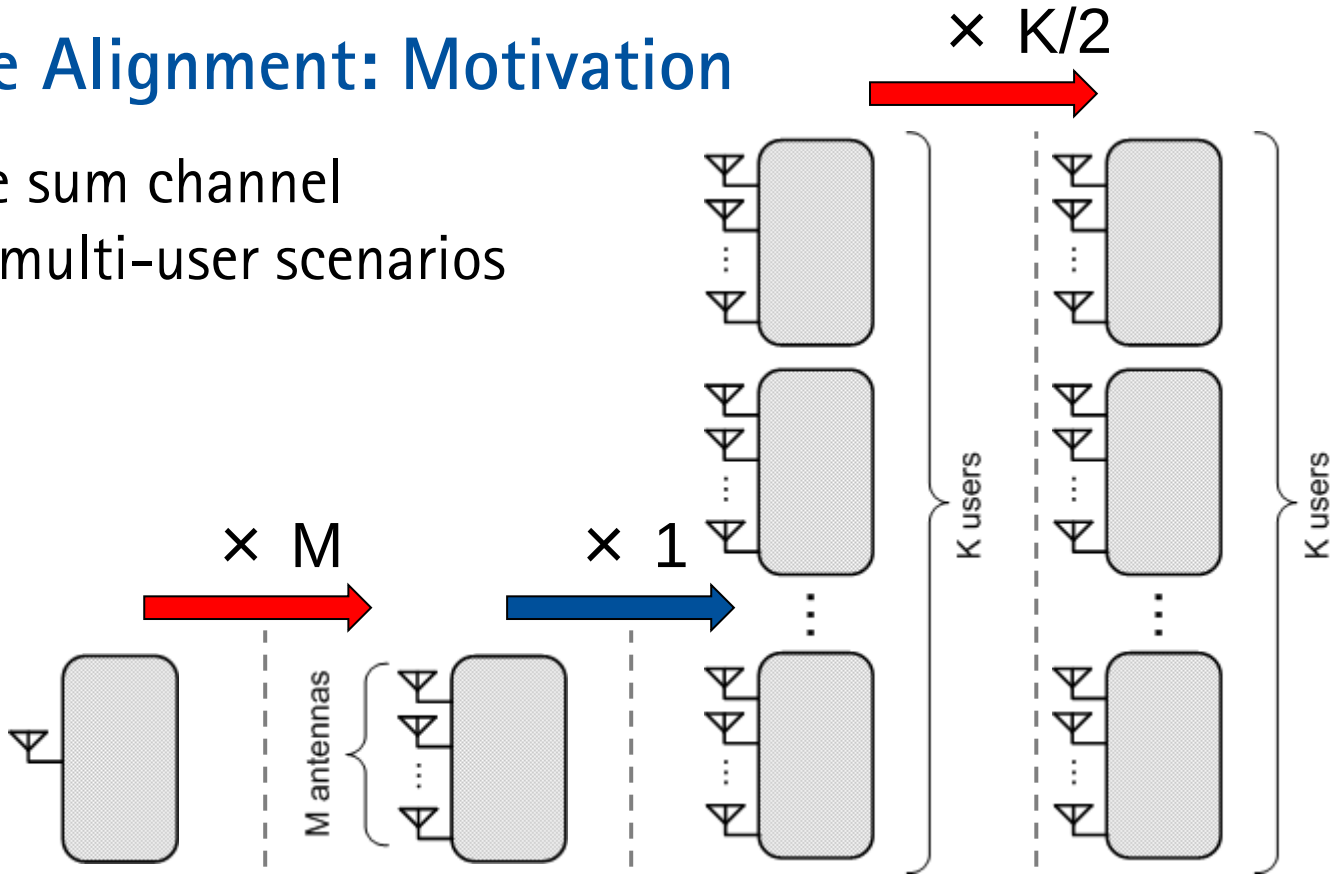


Outline

- Interference Alignment Hardware Acceleration
- Design Space Exploration Framework
- IA Case Study Implementation Results
- Conclusion

Interference Alignment: Motivation

Increasing the sum channel capacity C in multi-user scenarios

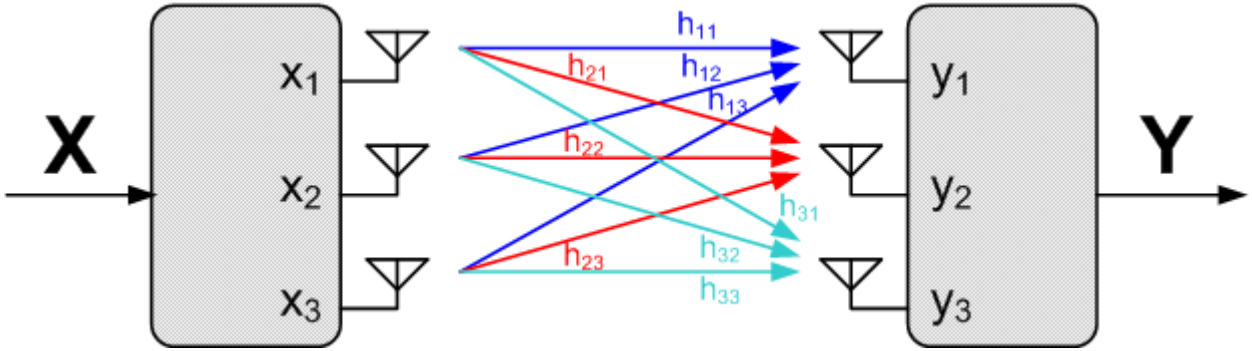


System	SISO	MIMO	MU-MIMO, **TDMA**	MU-MIMO, **IA**
Σ C	C_0	$M \cdot C_0$	$M \cdot C_0$	$K / 2 \cdot M \cdot C_0$
C per user	C_0	$M \cdot C_0$	$1 / K \cdot M \cdot C_0$	$1 / 2 \cdot M \cdot C_0$

B. Nazer, M. Gastpar, S. A. Jafar and S. Vishwanath, "Interference Alignment at Finite SNR: General Message Sets", 2009

Single User Spatial Multiplexing MIMO

- Multiple simultaneously transmitting antennas
- Multiple receiving antennas
- Linear superposition at receiver



$$\sum C = M \cdot C_0$$

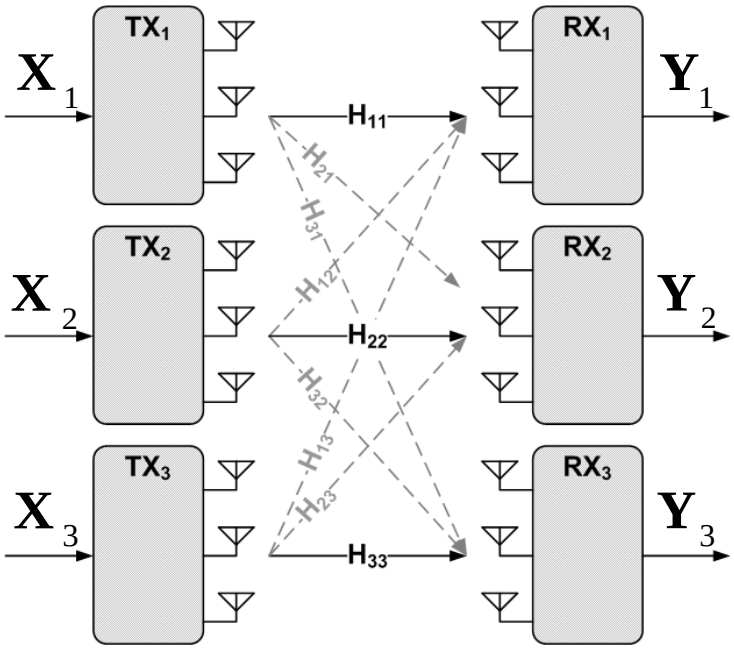
$$y_1 = h_{11}x_1 + h_{12}x_2 + h_{13}x_3$$

$$y_2 = h_{21}x_1 + h_{22}x_2 + h_{23}x_3$$

$$y_3 = h_{31}x_1 + h_{32}x_2 + h_{33}x_3$$

$$\mathbf{Y} = \mathbf{H}\,\mathbf{X}$$

Multi-User MIMO System



$$\sum C = M \cdot C_0$$

- Linear superposition at receiver

  → System of M linear equations in M·K unknowns

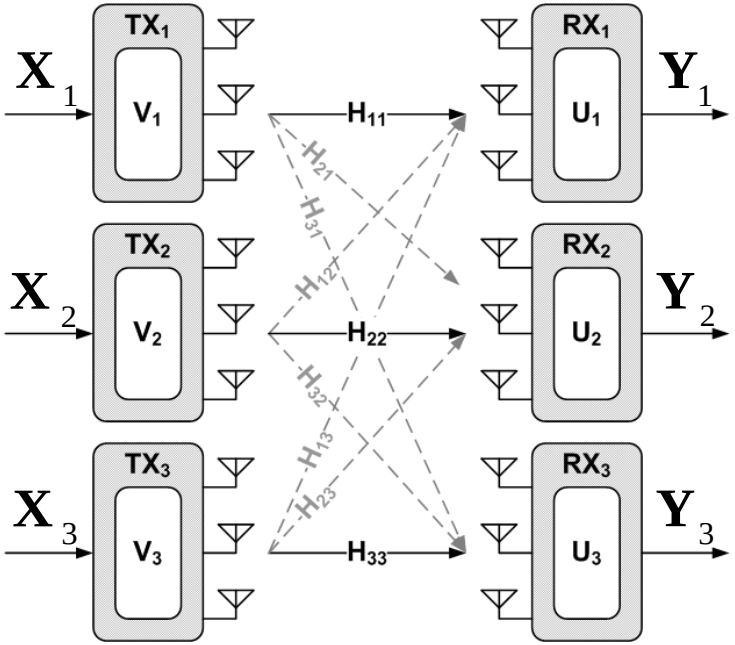
$$\mathbf{Y}_i = \sum_{j=1}^{K} \mathbf{H}_{ij} \mathbf{X}_j$$

- Problem: fewer observations than unknowns

  → underdetermined system

- IA approach: solve for subset of unknowns (desired signal), cancelling out all others (interference)

Interference Alignment Approach



$$\sum C = M \cdot C_0 \cdot \frac{K}{2}$$

- Insert linear precoding and decoding matrices $\mathbf{U}_i$ and $\mathbf{V}_i$

$$\mathbf{Y}_i = \mathbf{U}_i^T \left(\sum_{j=1}^{K} \mathbf{H}_{ij} \mathbf{V}_j \mathbf{X}_j \right)$$

- Sufficient conditions for perfect IA:

$$\hat{\mathbf{H}}_{ij} = \mathbf{U}_i^T \mathbf{H}_{ij} \mathbf{V}_j = \begin{cases} 0 & \forall\, i \neq j \\ I & \text{else} \end{cases}$$

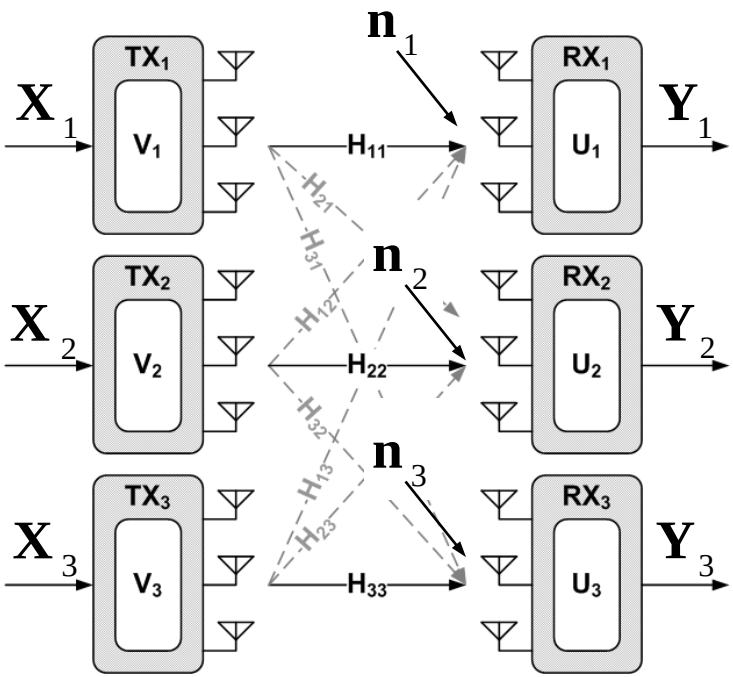
- Solve for $\mathbf{V}_j$ and $\mathbf{U}_i$

➡ Align all interference into the same subspace

What about noise?

V. Cadambe and S. Jafar, "Interference alignment and degrees of freedom of the K-user interference channel", 2008

Interference Alignment with Noise



- Consider noise at the receiver:

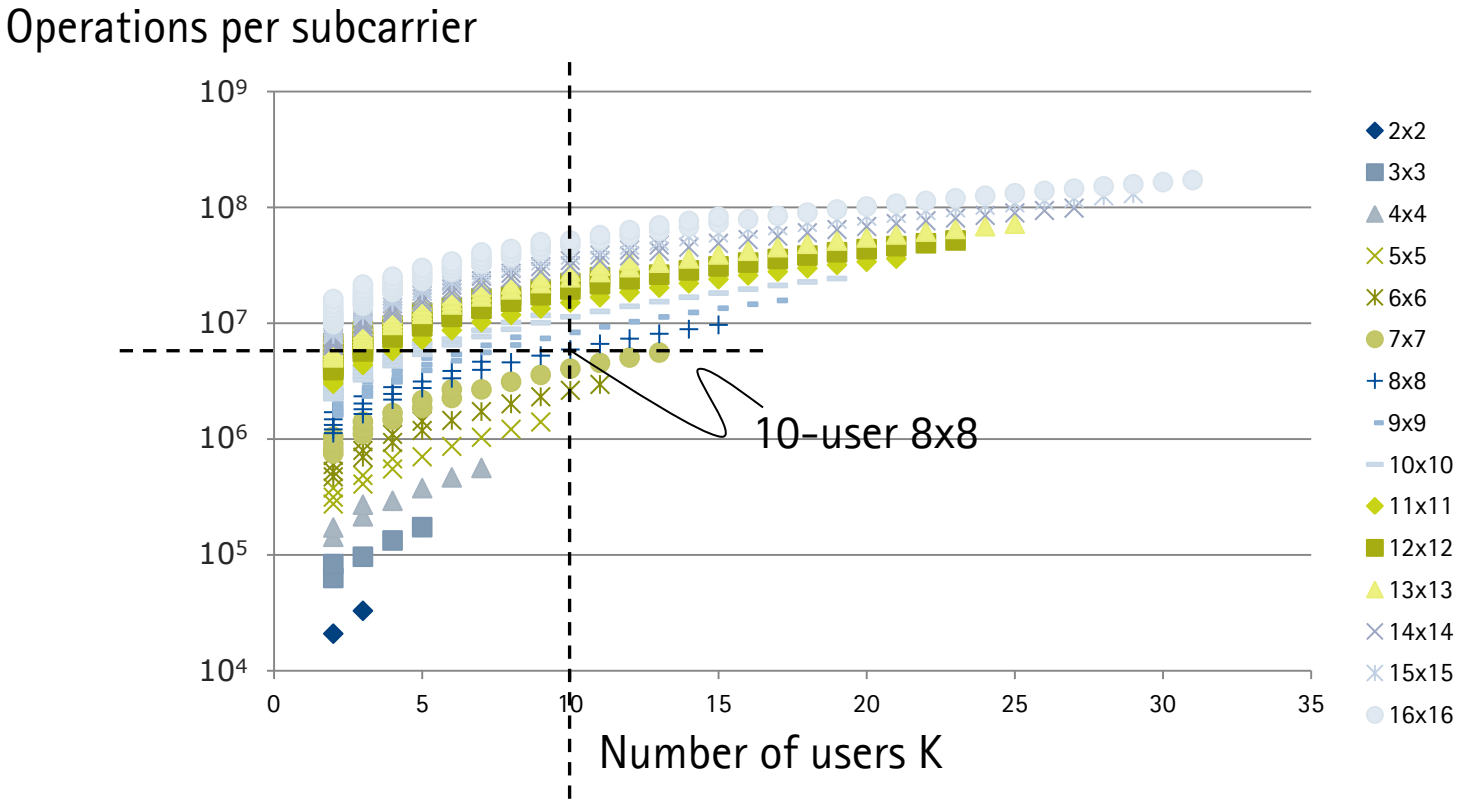
$$\mathbf{Y}_i = \mathbf{U}_i^T \left(\sum_{j=1}^{K} \mathbf{H}_{ij} \mathbf{V}_j \mathbf{X}_j + \mathbf{n}_i \right)$$

- ➔ Perfect IA is no longer the optimal solution
- MMSE criterion: minimize interference+noise

➡ **Numerically solve V_j and U_i for a given channel H and noise**

- Special cases: closed-form solutions available
- General case : iterative computation

Computational Complexity of Iterative MMSE IA

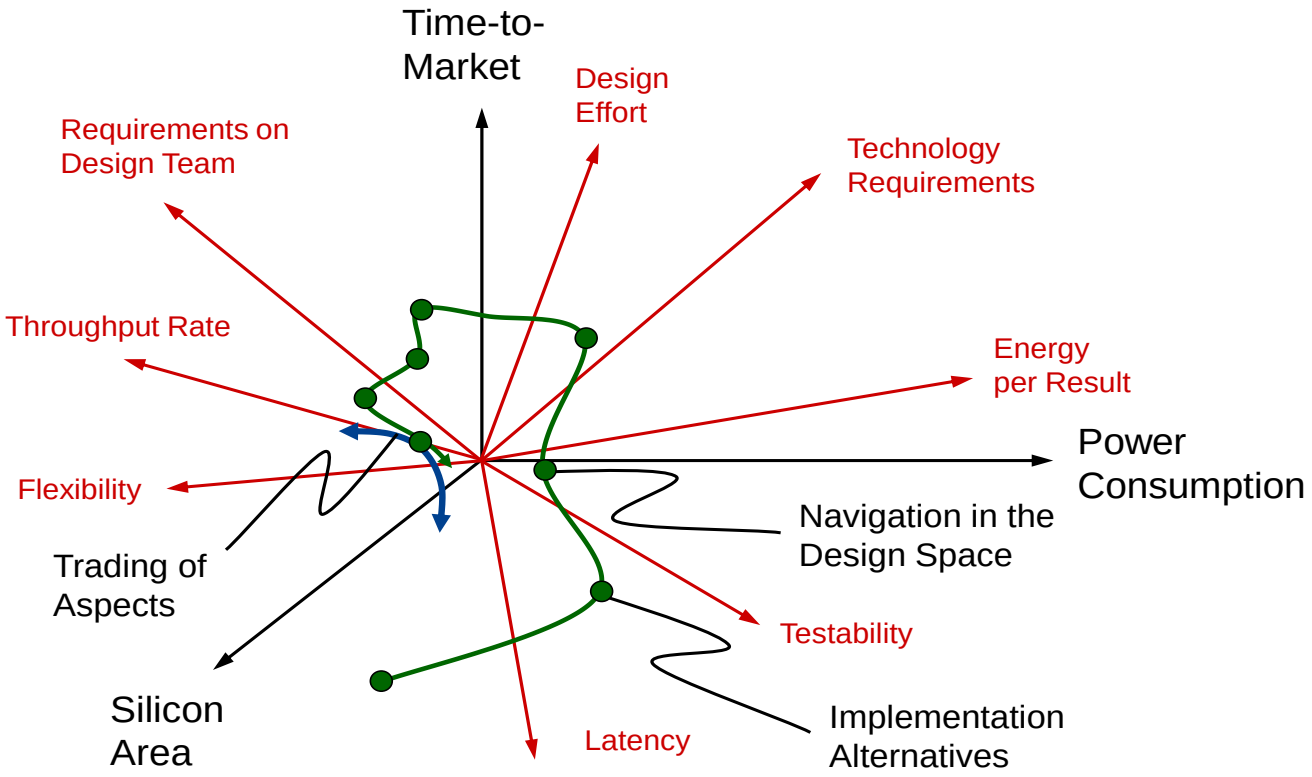


128 subcarrier OFDM system, 1ms latency ➔ 10^{12} Ops/sec

➡ Efficient hardware platforms for mobile applications needed

Design Space Exploration

How to choose design parameters for an efficient architecture?



Source: Noll, 2004

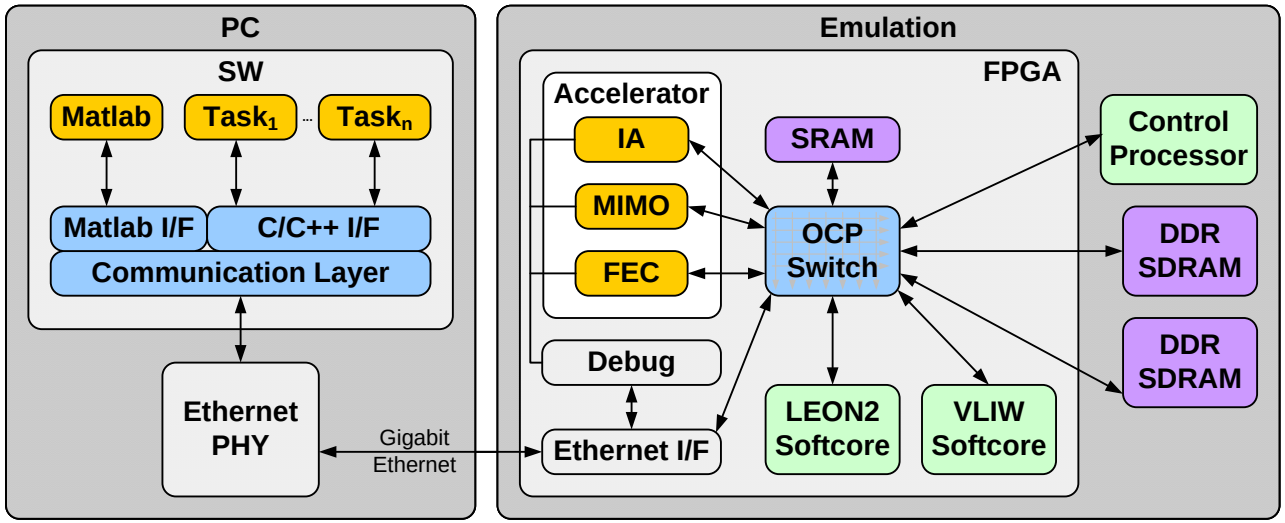
Identify relationship
between design parameters and characteristics of solution

DSE for Communication Systems

- How to obtain the model?
- Design and characterize different implementations
  - Possible parameter sets: degree of parallelism, wordlength, ...
  - Characterization:
    - Simulation
      - Too slow → use hardware acceleration
    - Use instrumented optimized target module for DSE
      - No separate simulation acceleration system needed

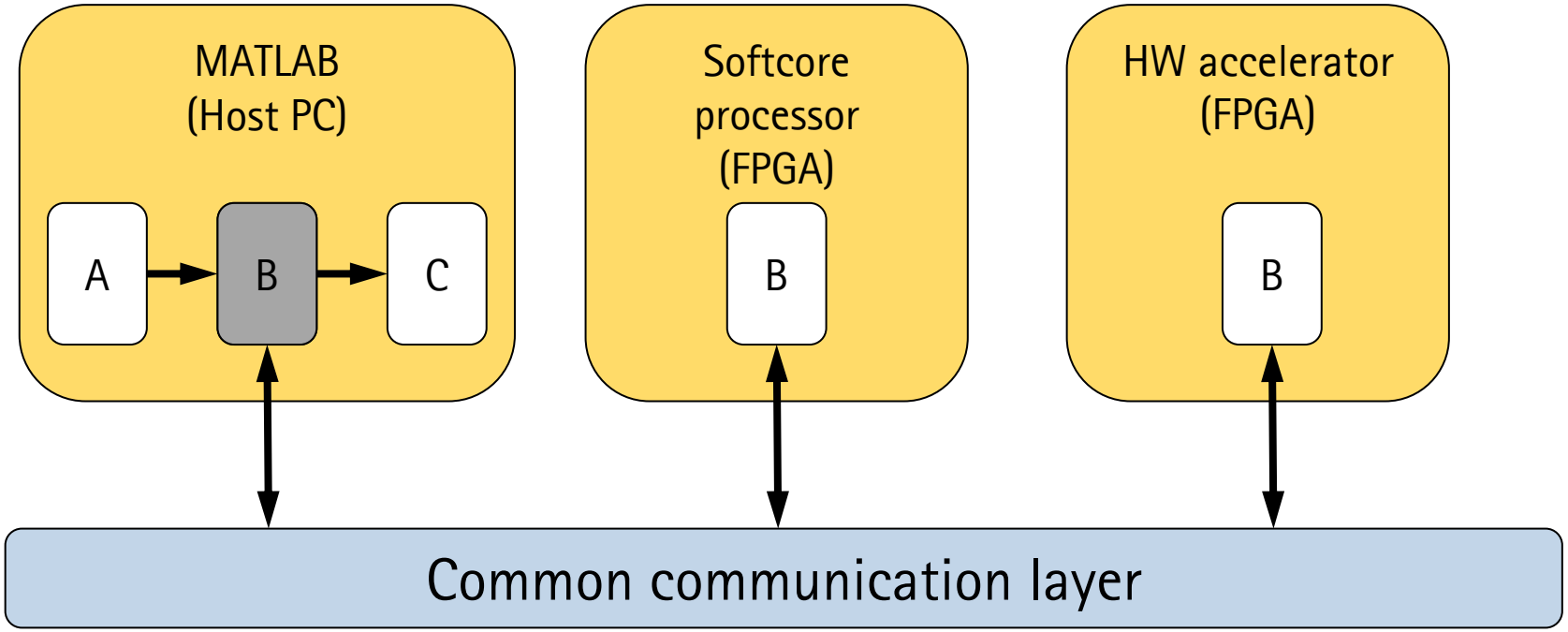
DSE Framework

- Typical System-on-Chip infrastructure template
- ASIC-inspired design
- DSE specific extensions and debug facilities
- Heterogeneous software/hardware co-verification and simulation



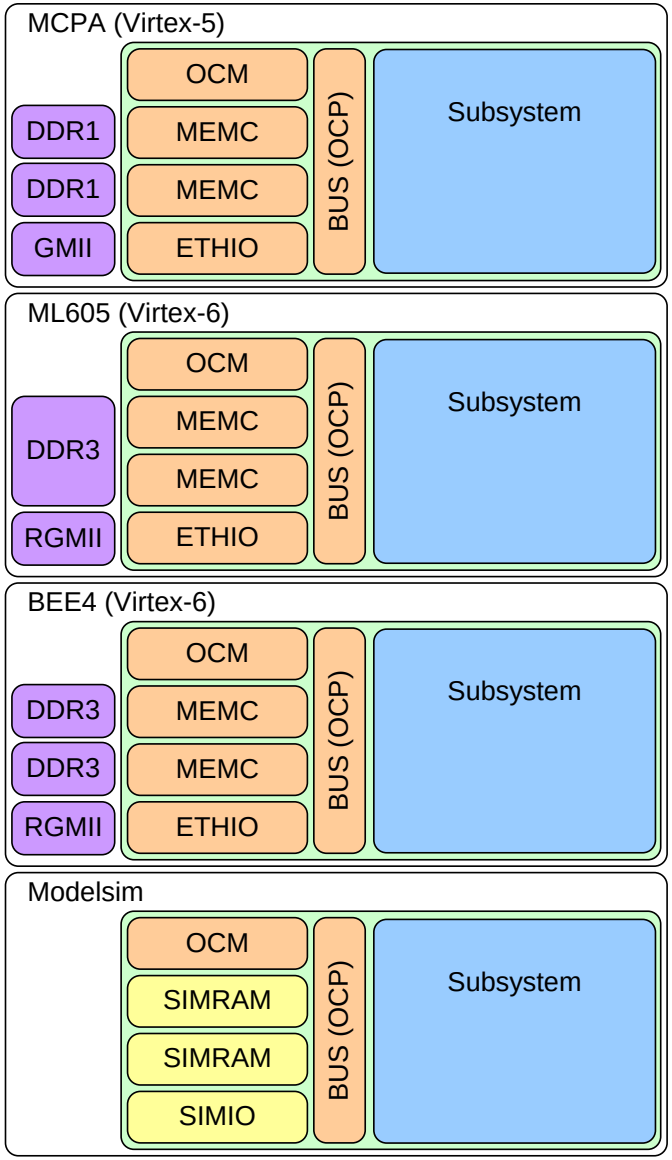
Flat Communication Hierarchy

- Freely move signal processing blocks between resources
  - Implement / verify single blocks in full system context



Multi-Target HW Design

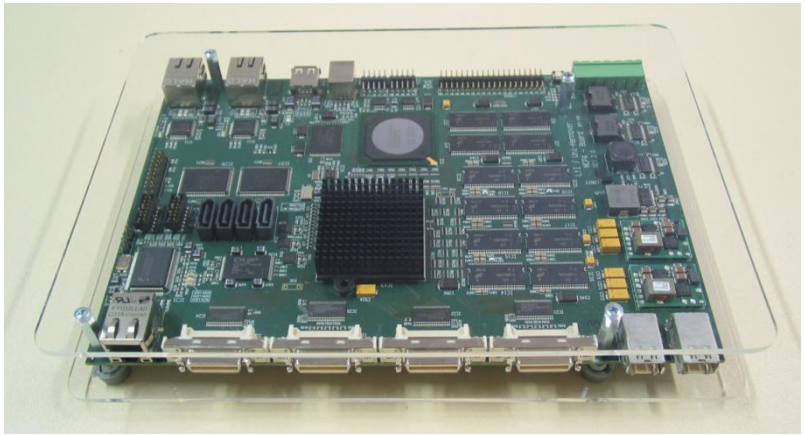
- Targets: Emulation systems, simulation, (ASIC)
- Wrappers encapsulate target specifics
- Application-specific subsystem
  - Target-independent interfaces
- Silicon-proven infrastructure
- Collaboration: test and verify individual blocks on commodity HW
- Upcoming support for more targets
  - VC707
  - Zynq



Case Study: 3-User 2x3 MIMO with Antenna Selection

- Zero-Forcing IA
- Select best 2 out of 3 antennas
- Compute V, U for each combination
- Hardwired integer accelerator
- Example system:
  - 128 subcarrier OFDM
  - max. 1 ms latency

➔Requires: 2.8 GOPS



MPCA emulator board
Virtex-5 LX220T FPGA, 2x256 MB DDR1 RAM

OP	ADD	MUL	SQR	SQRT	1/SQRT
Count	506	249	34	6	1

Operations required to compute one set of V, U and R

Matlab Xeon 2.4 GHz CPU	3.63 s
MCPA Emulator board @ 100 MHz	380 µs

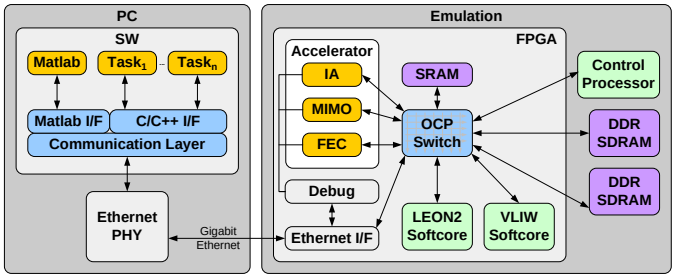
Runtime comparison

Summary

- Interference alignment
  - MMSE-IA computational complexity
- DSE approach built on optimized target implementation
  - Multi-target framework
- IA acceleration case study

Conclusion

- Using instrumented target implementation for DSE reduces overall design time



- Joint research on IA algorithms and HW architectures required

Thank you for your attention!